Monte Carlo and Corners Simulations: Verifying Effectively and Efficiently Pre-Si

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Context

- With continued scaling of MOSFETs, variation has become a very important issue.
- This issue becomes particularly important in sub-threshold, where a thorough and accurate assessment of variation robustness pre-Si is vital.
- Monte Carlo (MC) and Corners analyses are often run in order to simulate variations from the manufacturing process.

Context (2)

Problems with these approaches:

- Running a meaningful number of Monte Carlo (MC) seeds is very time consuming.
- Running process corners analyses can be inadequate or overkill depending on the methodology used.
- Results from these simulations are often described qualitatively rather than quantitatively.
- There is little consensus on the optimal approach for running MC simulations.
  - By optimal I mean enough seeds to have useful information about the robustness of a circuit, but not so many that a circuit cannot be fully tested due to time constraints.
  - The other potential issue in running too many seeds is irrelevant anomalies (i.e. if you run something long enough, anything could happen).

Previous Work [1]

[1]

- Presents an algorithm to compute the distribution of circuit delay by treating parameters impacted by process variations as random variables with different levels of correlatedness
- Shows that simulating multiple process corners often overestimates the standard deviation

[2]

- Analyzes relationship between statistical and process-induced variations for FinFETs in 14nm SOI

Previous Work [3]

- Patented Jan. 2014
- Variations are typically characterized qualitatively rather than quantitatively
- Developed and patented a computer model based scheme to quantitatively describe the probabilities of process variations
- More accurately consider manufacturing variations—each parameter is modeled as a different distribution function (Fig. 2)
- Uses process MC simulations

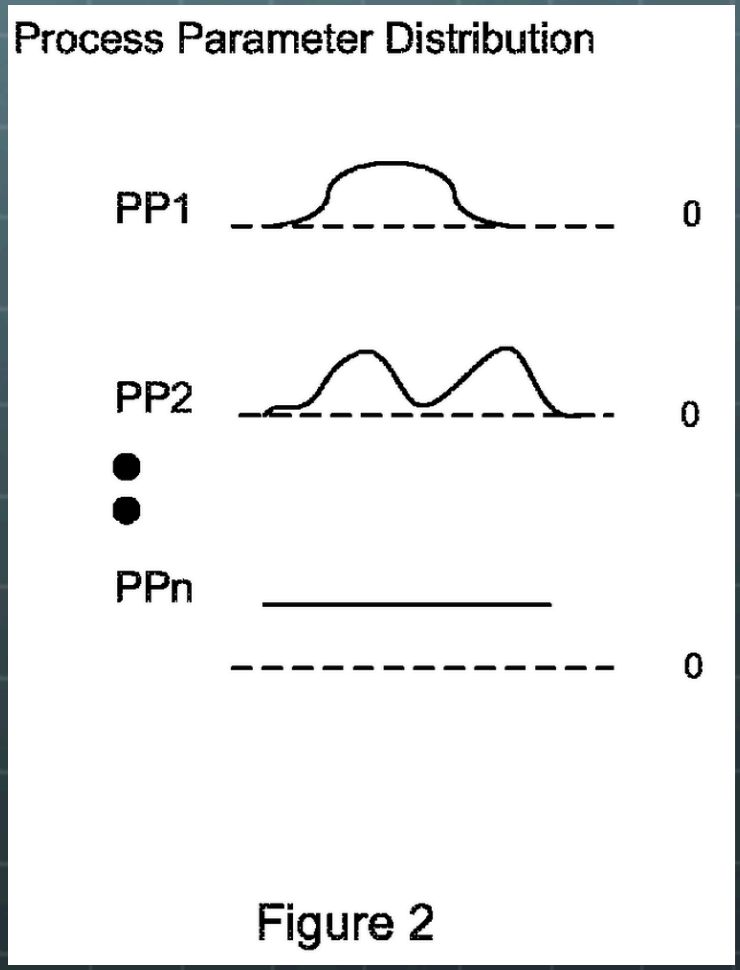

Figure 2

[3] Mehrotra, et al.

Problem Statement

- How can we most efficiently and effectively test a circuit's robustness pre-Si?
  - In testing circuit components, how do we balance the effectiveness of simulating with MC and the efficiency of simulating with Corners?
  - Is there a way to accomplish the same thing with fewer seeds or with another kind of simulation?

Conceptual Approach

- What does the data from a Corners simulation tell you about a MC simulation and vice versa?
- How do we isolate the "tail" seeds generated by a MC simulation? If we could do this, it would save time since these "worst case" seeds are what we are really interested in.
  - Can we get this information from running Corners analyses?
  - Is simulating process corners enough? If not, how can we use what we learn from a Corners simulation to reduce the time spent simulating our circuit with MC?

Implementing Approach

- Run Corners and MC analyses on ring oscillators (ROs), varying size, temperature, and VDD
  - Inverter
  - 2-input NAND and NOR
  - 2-to-1 mux
- See if I can map results from each simulation type to the other (i.e. results from Corners to MC and vice versa)

Results

- I expect Corners simulations to identify the “tail” cases of MC
- Therefore, I expect circuit behavior at worst case process corners to be a good indicator of circuit robustness
- Deliverables:
  - Plots from MC and Corners simulations
  - A generally applicable and quantifiable way of mapping from Corners simulations to MC simulations (and/or vice versa)

Milestones

For Project Report 1 on 3/3:

- Run Corners simulations on
  - 9, 25, and 49 device ROs at 0, 27, and 100 degrees Celsius sweeping VDD from 150mV to 1V

For Project Report 2 on 3/24:

- Run MC simulations on
  - 9, 25, and 49 device ROs at 0, 27, and 100 degrees Celsius sweeping VDD from 150mV to 1V

For final report:

- Compare simulation results and identify a mapping

References

[1] Chang, Hongliang, and Sachin S. Sapatnekar. "Statistical timing analysis considering spatial correlations using a single PERT-like traversal."*Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design*. IEEE Computer Society, 2003.

[2] Wang, Xingsheng, et al. "Interplay between process-induced and statistical variability in 14-nm CMOS technology double-gate SOI FinFETs." *Electron Devices, IEEE Transactions on* 60.8 (2013): 2485-2492.

[3] Mehrotra, Amit, et al. "Circuit instance variation probability system and method." U.S. Patent No. 8,631,362. 14 Jan. 2014.

Thank you!

- Questions?
- Comments?
- Feedback on this topic?